What is claimed is.

1. An address pattern generator comprising a column address generator for receiving an add signal from a control circuit, an address value from a first maximum value register and an address value from a first initial-value register and a row address generator for receiving an add signal from the control circuit, an address value from a second maximum value register and an address value from a second initial-value register, characterized in that the arrangement of said column address generator is the same as that of said row address generator and said column address generator comprises a comparator for comparing an address signal to be supplied to a memory to be tested with said address value output from said first maximum value register and a selection circuit for switching address signals to be supplied to said memory using a signal output from said comparator.

add A2

13